FIG. 1 DIFFERENTIAL SIGNAL OUTPUT CIRCUIT IN FIRST EMBODIMENT

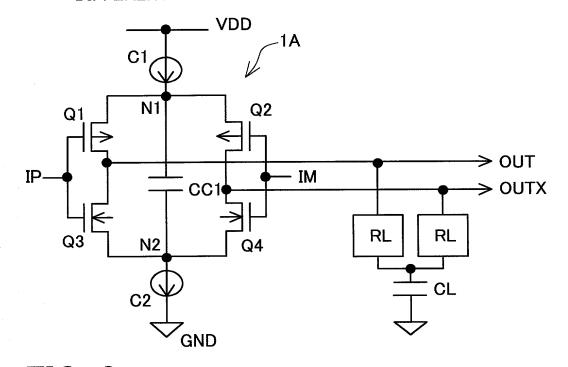


FIG. 2

EXAMPLE OF CURRENT SOURCE IN FIRST EMBODIMENT

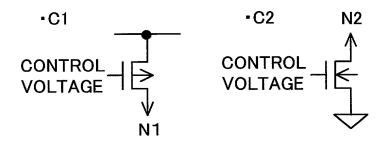


FIG. 3

SPECIFIC EXAMPLE OF CAPACITOR IN FIRST EMBODIMENT



FIG. 4
SPECIFIC EXAMPLE IN FIRST EMBODIMENT

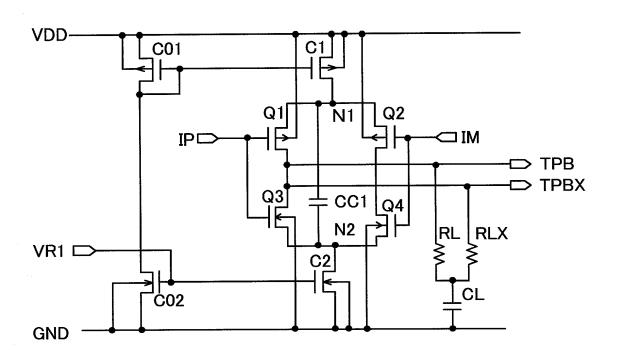


FIG. 5A

DIFFERENTIAL OUTPUT WAVEFORMS ACCORDING TO RESULT OF SIMULATION OF SPECIFIC EXAMPLE OF FIRST EMBODIMENT

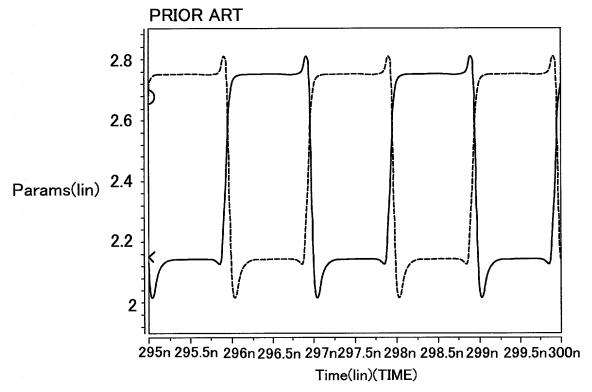
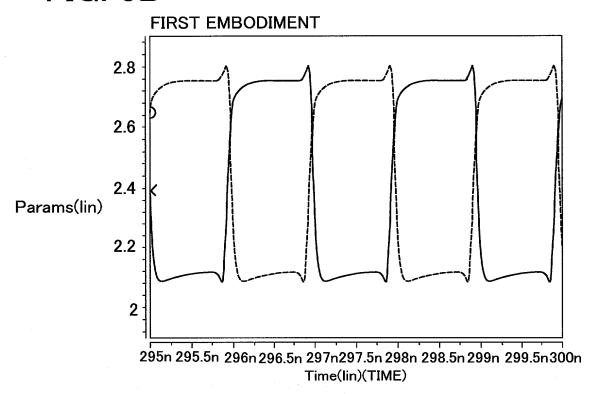


FIG. 5B



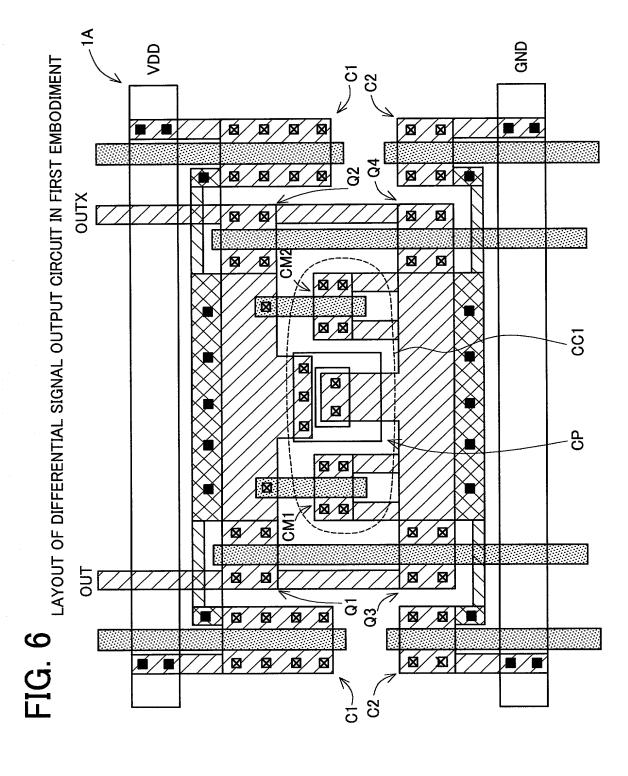


FIG. 7A

DIFFERENTIAL SIGNAL OUTPUT CIRCUIT IN SECOND EMBODIMENT

CIRCUIT STRUCTURED WITH PASSIVE LOADS

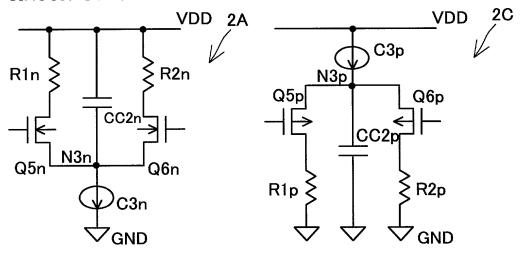


FIG. 7B

CIRCUIT STRUCTURED WITH ACTIVE LOADS

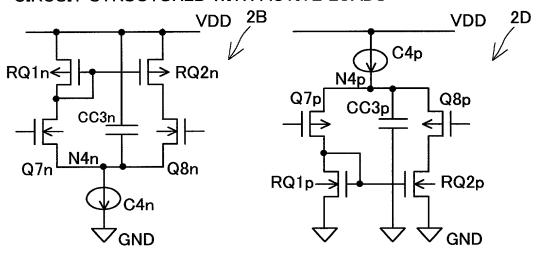


FIG. 8

BLOCK DIAGRAM ILLUSTRATING SIGNAL DETECTION APPARATUS IN THIRD EMBODIMENT

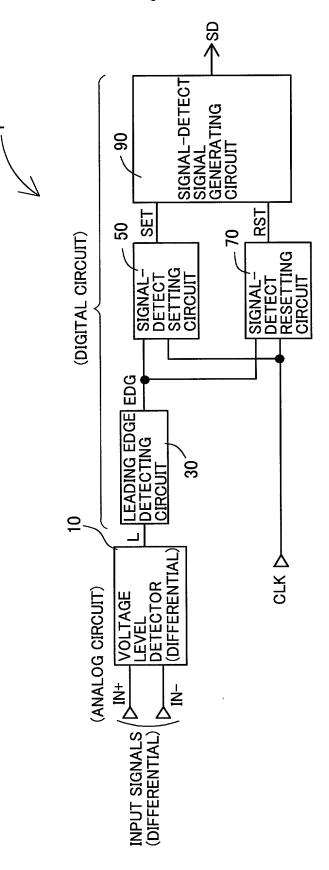
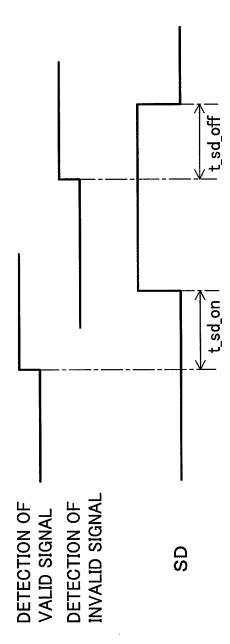


FIG. 9

TIMING PARAMETERS OF SIGNAL-DETECT SIGNALS ACCORDING TO P1394b STANDARD



SYMBOL	PARAMETER	LIND	MIN	UNIT MIN. MAX.
+ cd on	DELAY TIME FROM DETECTION OF A VALID SIGNAL UNTIL	π sec	ı	100
5	ASSERTION OF A SIGNAL-DETECT SIGNAL			8
Ho ho +	DELAY TIME FROM DETECTION OF AN INVALID SIGNAL UNTIL $\mu \sec$	η sec	ı	t_sd_on
5	NAGATION OF A SIGNAL-DETECT SIGNAL			

FIG. 10 CODE TABLE(1)
8b10bCODES ACCORDING TO P1394b STANDARD

		<u> </u>		00100000			J F 10840 01	
	INP			GHJ OUTPUT		INPUT	ABCDEI FGHJ	
NAME	A'B'C	<u>''D'E'F'G'H'</u>	RD<0	RD>0	NAME	A'B'C'D'E'F'G'H'	RD<0	RD>0
BO O	NANC	1		[I] [0] DATA_TAB		1		DATA_TABLE[I][1]
		00000	1001110100			00100000	1101010100	0010101011
		00001	1001110010			00100001		0010101101
		0010	1001110101	01100001		00100010	1101010101	0010100101
		0011	1001110110	01100001		00100011	1101010110	0010100110
		00100	1001111001	01100010		00100100	1101011001	0010101001
		00101	1001111010	01100010			1101011010	0010101010
		0110	1001110011	01100011			1101010011	0010101100
		0111	1001110001	01100011		00100111		0010101110
D16.0			0110110100	10010010			0010111011	0010110100
D16.4			0110110010			00101001		0010110010
D16.2			0110110101	10010001				0010110101
D16.6	0000	1011	0110110110	10010001				0010110110
D16.1			0110111001	10010010				0010111001
D16.5	0000	1101	0110111010	10010010				0010111010
D16.3	0000)1110	0110110011	10010011			0010111100	0010110011
D16.7	0000	11111	0110110001	10010011			0010110111	0010110001
D8.0	0001	0000	1110010100	00011010			0011011011	0011010100
D8.4	0001	0001	1110010010	00011011			0011011101	0011010010
	0001	0010	1110010101	00011001		00110010		0011010101
D8.6	000	0011	1110010110	00011001			0011010110	0011010110
D8.1	0001	0100	1110011001	00011010	01 D12.1			0011011001
	0001	0101	1110011010	00011010				0011011010
		0110	1110010011	00011011	00 D12.3	00110110		0011010011
		0111	1110010001	00011011				0011010001
D24.0	0001	1000	1100110100	00110010		00111000	0011101011	0011100100
D24.4	0001	1001	1100110010	00110011	01 D28.4	00111001	0011101101	0011100010
D24.2			1100110101	001100010			0011100101	0011100101
D24.6			1100110110	00110001			0011100110	0011100110
D24.1			1100111001	00110010			0011101001	0011101001
D24.5			1100111010	00110010			0011101010	0011101010
D24.3			1100110011	001100110			0011101100	0011100011
D24.7			1100110001	00110011			0011101110	0011100001
D2.0	0100	00000	1011010100	01001010	1 D6.0			0110010100
D2.4	0100	00001	1011010010	01001011	01 D6.4	01100001	0110011101	0110010010
		00010	1011010101	01001001	<i>01</i> D6.2	01100010	0110010101	0110010101
D2.6	0100	00011	1011010110	01001001	0 D6.6	01100011	0110010110	0110010110
D2.1	0100	00100	1011011001	01001010	<i>D1</i> D6.1	01100100	0110011001	0110011001
			1011011010	01001010	70 D6.5	01100101	0110011010	0110011010
	0100	0110	1011010011	010010116			0110011100	0110010011
D2.7	0100	10111	1011010001	01001011	0 D6.7	01100111	0110011110	0110010001
D18.0	0100	1000	0100111011	010011010	00 D22.0	01101000	0110101011	0110100100
D18.4			0100111101	01001100	0 D22.4	01101001	0110101101	0110100010
D18.2	0100	1,010	0100110101	010011010				0110100101
D18.6			0100110110	01001101	0 D22.6	01101011	0110100110	0110100110
D18.1			0100111001	01001110				0110101001
D18.5	0100	1101	0100111010	01001110		01101101	0110101010	0110101010
D18.3	0100	01110	0100111100	01001100				0110100011
D18.7	0100	1111	0100110111	010011000)1 D22.7	01101111		0110100001
D10.0			0101011011	01010101	<i>00</i> D14.0	01110000		0111000100
D10.4	0101	0001	0101011101	01010100	70 D14.4	01110001	0111001101	0111000010
D10.2			(1)(1)(1)(1)(1)(1)			01110010		0111000101
D10.6			0101010110	01010101		01110011		0111000110
D10.1	0101	0100	0101011001	010101100				0111001001
D10.5	0101	0101	0101011010	01010110	0 D14.5	01110101		0111001010
D10.3	0101	0110	0101011100	01010100				0111000011
D10.7	0101	0111	0101011110	01010100				0111001000
D26.0			0101101011	010110010				1000011011
D26.4			0101101101	01011000				1000011101
D26.2	0101		0101100101	010110010		01111010		1000010101
D26.6			0101100110	01011001				1000010110
D26.1			0101101001	010110100				1000011001
D26.5			0101101010	01011010				1000011010
D26.3			0101101100	010110001				1000011100
D26.7			0101101110	010110000				1000011110
D1.0			0111010100	10001010				1010010100
			0111010010	100010110				1010010010
			0111010101	10001001				1010010010
			0111010110	10001001				1010010110
للتنت					- [

FIG. 11 CODE TABLE(2)
8b10bCODES ACCORDING TO P1394b STANDARD

<u> 114.</u>			CCORDING TO		
INPUT	ABCDEI FGHJ		INPUT	ABCDEI FGH	
NAME A'B'C'D'E'F'G'H'	RD<0		NAME A'B'C'D'E'F'G'H		RD>0
Table 1	DATA_TABLE[I] [0]	DATA_TABLE[I][1]	l l	DATA_TABLE[I] [0]	DATA_TABLE[I] [1]
D1.1 10000100	0111011001	1000101001	D5.1 10100100	1010011001	1010011001
D1.5 10000101	0111011010	1000101010	D5.5 10100101	1010011010	1010011010
D1.3 10000110	0111010011	1000101100	D5.3 10100110	1010011100	1010010011
D1.7 10000111	0111010001	1000101110	D5.7 10100111	1010011110	1010010001
D17.0 10001000	1000111011	1000110100	D21.0 10101000	1010101011	1010100100
D17.4 10001001	1000111101	1000110010	D21.4 10101001	1010101101	1010100010
D17.2 10001010	1000110101	1000110101	D21.2 10101010	\$\$!\$\$!\$\$!!\$\$!	
D17.6 10001011	1000110110	1000110110	D21.6 10101011	1010100110	1010100110
D17.1110001100	1000111001	1000111001 1000111010	D21.1 10101100	86:36:36:36:36:36:3 86:36:36:36:36:36:3	######################################
D17.5 10001101	1000111010 1000111100	1000110011	D21.5 10101101 D21.3 10101110	1010101100	1010100011
D17.3 10001110 D17.7 10001111	1000111111	1000110011	D21.7 10101111	1010101110	1010100001
D9.0 10010000	1001011011	1001010100	D13.0 10110000	1011001011	1011000100
D9.4 10010001	1001011101	1001010010	D13.4 10110001	1011001101	101100010
D9.2 10010010	7.60.60.60.60.60.60.60.60.60.60.60.60.60.	# (U/U) (U) (U) (U)	D13.2 10110010	1011000101	1011000101
D9.6 10010011	1001010110	11001010110	D13.6 10110011	1011000110	1011000110
D9.1 10010100	1001011001	1001011001	D13.1 10110100	1011001001	1011001001
D9.5 10010101	1001011010	1001011010	D13.5 10110101	1011001010	1011001010
D9.3 10010110	1001011100	1001010011	D13.3 10110110	1011001100	1011000011
D9.7 10010111	1001011110	1001010001	D13.7 10110111	1011001110	1011001000
D25.0 10011000	1001101011	1001100100	D29.0 10111000	1011100100	0100011011
D25.4 10011001	1001101101	1001100010	D29.4 10111001	1011100010	0100011101
D25.2 10011010	1001100101	1001100101	D29.2 10111010	1011100101	0100010101
D25.6 10011011	1001100110	1001100110	D29.6 10111011	1011100110	0100010110
D25.1 10011100	1001101001	1001101001	D29.1 10111100	1011101001	0100011001
D25.5 10011101	1001101010	1001101010 1001100011	D29.5 10111101 D29.3 10111110	1011101010 1011100011	0100011010 0100011100
D25.3 10011110 D25.7 10011111	1001101100 1001101110	1001100011	D29.7 10111111	1011100001	0100011110
D3.0 11000000	1100011011	1100010100	D7.0 111100000	1110001011	0001110100
D3.4 111000001	1100011101	1100010010	D7.4 111100001	1110001101	0001110010
D3.2 11000010	1100010101	1100010101	D7.2 111100010	1110000101	0001110101
D3.6 11000011	1100010110	1100010110	D7.6 11100011	1110000110	0001110110
D3.1 11000100	1100011001	1100011001	D7.1 11100100	1110001001	0001111001
D3.5 11000101	1100011010	1100011010	D7.5 11100101	1110001010	0001111010
D3.3 [11000110	111000111100	1100010011	D7.3 11100110		0001110011
D3.7 11000111	1100011110	1100010001	D7.7 11100111	1110001110	0001110001
D19.0 11001000	1100101011	1100100100	D23.0 11101000	1110100100	0001011011
D19.4 11001001	1100101101	1100100010	D23.4 11101001	1110100010	0001011101
D19.2 11001010	1100100101	1100100101	D23.2 11101010	1110100101	0001010101
D19.6 11001011	1100100110	1100100110	D23.6 11101011	1110100110	0001010110
D19.1 11001100	1100101001	1100101001	D23.1 11101100	1110101001	0001011001
D19.5 11001101	1100101010	1100101010	D23.5 11101101	1110101010	0001011010
D19.3 11001110	1100101100	1100100011	D23.3 11101110	1110100011	0001011100
D19.7 11001111	1100101110	1100100011	D23.7 11101111	1110100001	0001011110
D11.0 11010000		1101000100	D15.0 11110000	0101110100	
	1101001011				1010001011
D11.4 11010001	1101001101	1101000010	D15.4 11110001	0101110010	1010001101
D11.2 11010010	1101000101	1101000101	D15.2 11110010	0101110101	1010000101
D11.6 11010011	1101000110	1101000110	D15.6 11110011	0101110110	1010000110
D11.1 11010100	1101001001	1101001001	D15.1 11110100	0101111001	1010001001
D11.5 11010101	1101001010	1101001010	D15.5 11110101	0101111010	1010001010
D11.3 11010110	1101001100		D15.3 11110110	0101110011	1010001100
D11.7 11010111	1101001110		D15.7 11110111	0101110001	1010001110
D27.0 11011000	1101100100		D31.0 11111000	1010110100	0101001011
D27.4 11011001	1101100010		D31.4 11111001	1010110010	0101001101
D27.2 11011010	1101100101	0010010101	D31.2 11111010	1010110101	0101000101
D27.6 11011011	1101100110	0010010110	D31.6 11111011	1010110110	0101000110
D27.1 11011100	1101101001		D31.1 111111100	1010111001	0101001001
D27.5 11011101	1101101010		D31.5 11111101	1010111010	0101001010
D27.3 11011110	1101100011		D31.3 11111110		0101001100
D27.7 11011111	1101100001	0010011110	D31.7 111111111	1010110001	0101001110

FIG. 12

SPECIFIC EXAMPLE VOLTAGE LEVEL DETECTOR IN THIRD EMBODIMENT

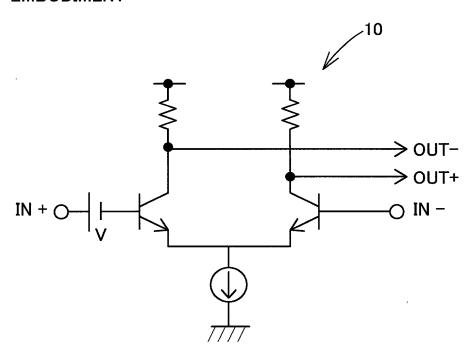


FIG. 13

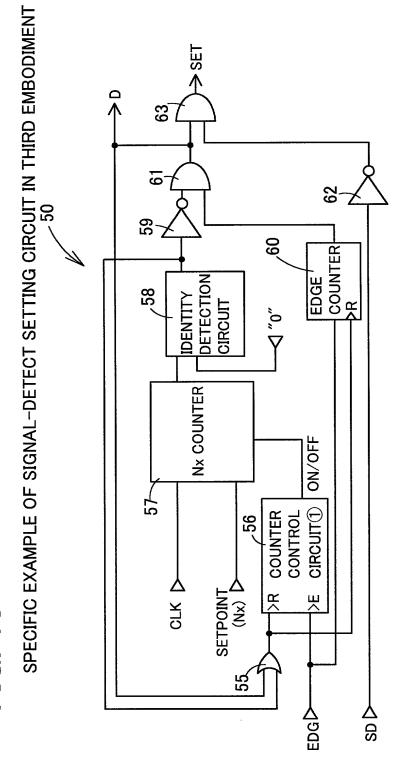


FIG. 14

SPECIFIC EXAMPLE OF SIGNAL-DETECT RESETTING CIRCUIT IN THIRD EMBODIMENT

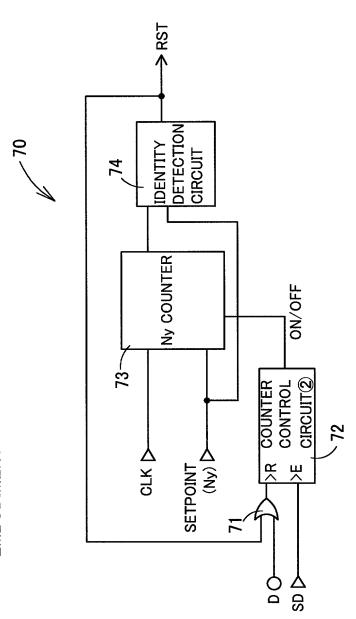


FIG. 15 SIGNAL-DETECT SIGNAL SETTING SEQUENCE

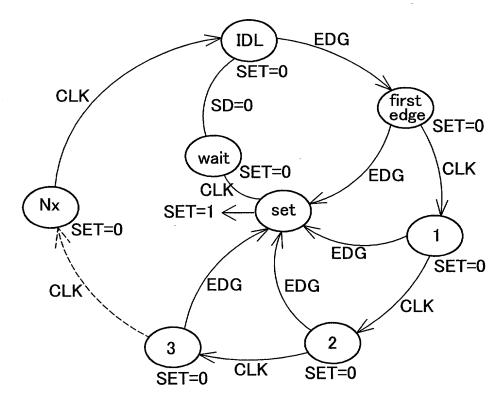


FIG. 16 SIGNAL-DETECT SIGNAL RESETTING SEQUENCE

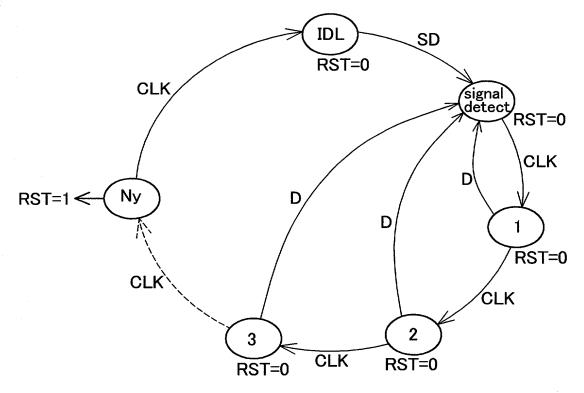
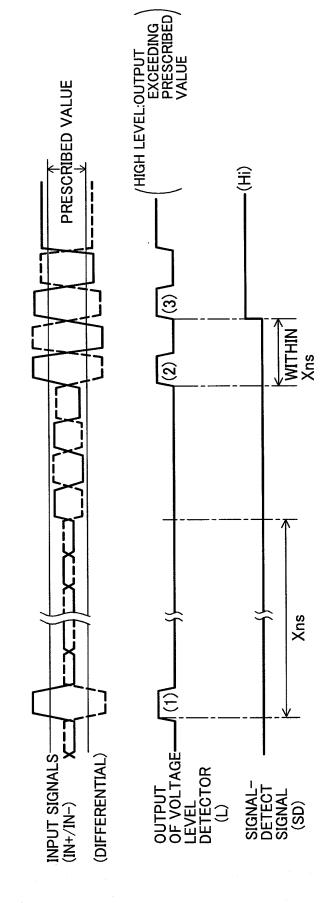


FIG. 17

TIME CHART SHOWING SIGNAL-DETECT SIGNAL SETTING SEQUENCE



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FIG. 18

TIME CHART SHOWING ACTIONS DURING SIGNAL-DETECT SIGNAL SETTING

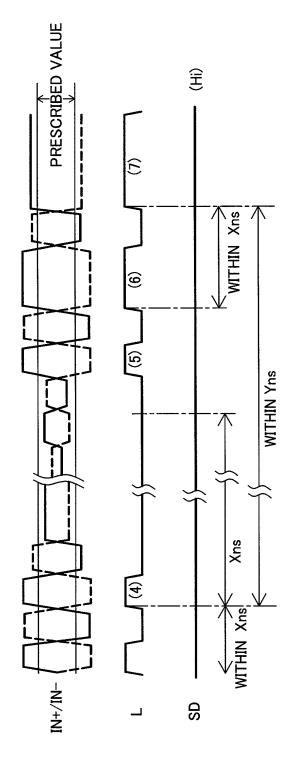


FIG. 19

TIME CHART SHOWING SIGNAL-DETECT SIGNAL RESETTING SEQUENCE

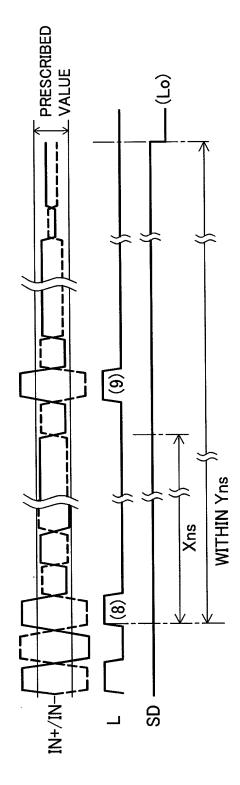


FIG. 20

CONFIGURATIONAL DIAGRAM OF SIGNAL DETECTION APPARATUS IN FOURTH EMBODIMENT

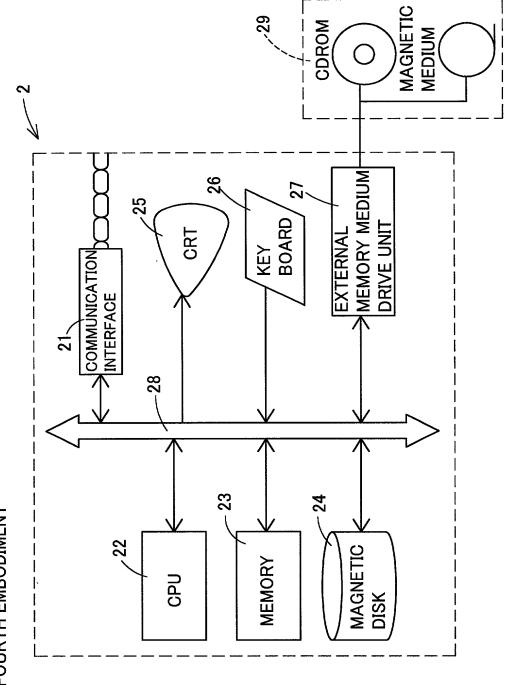


FIG. 21 SIGNAL DETECTION METHOD EXECUTED BY SIGNAL DETECTION APPARATUS IN FOURTH EMBODIMENT

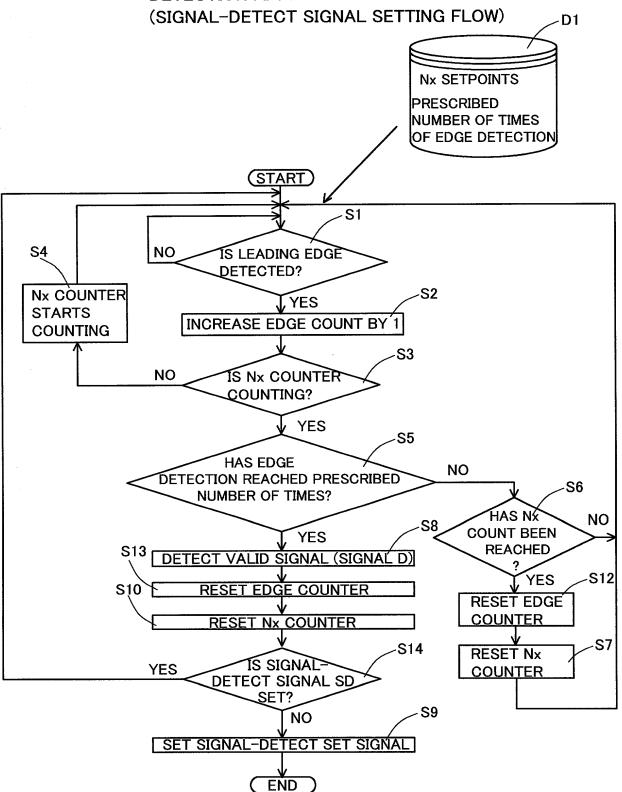


FIG. 22 SIGNAL DETECTION METHOD EXECUTED BY SIGNAL DETECTION APPARATUS IN FOURTH EMBODIMENT (SIGNAL-DETECT SIGNAL RESETTING FLOW)

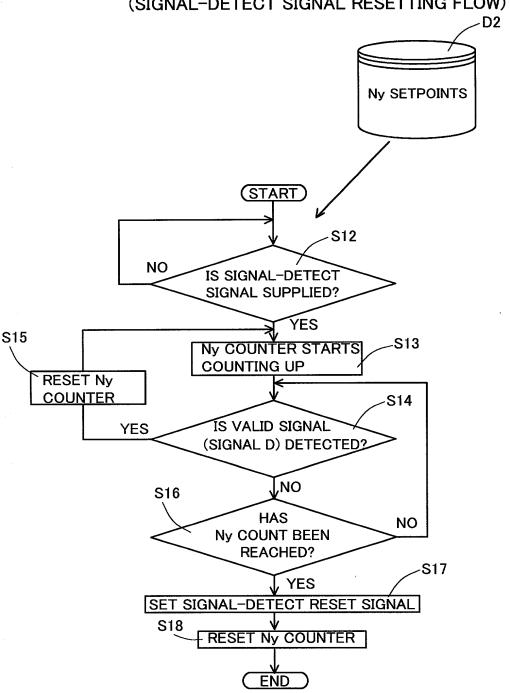


FIG. 23

EXAMPLE OF DIFFERENTIAL SIGNAL TRANSMISSION SYSTEM

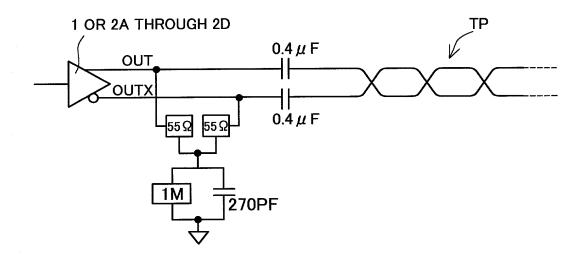


FIG. 24

EXAMPLE OF SIGNAL TRANSMISSION SYSTEM CONFIGULATION

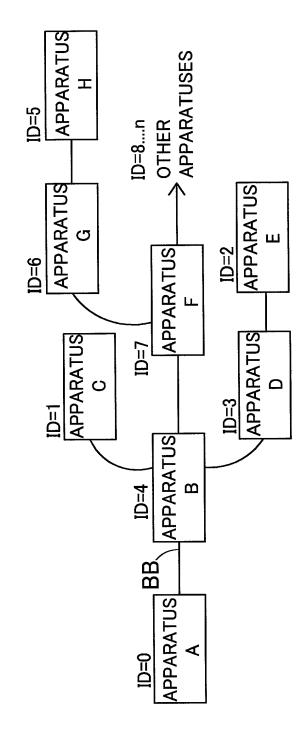


FIG. 25 PRIOR ART

DIFFERENTIAL SIGNAL OUTPUT CIRCUIT ACCORDING TO PRIOR ART

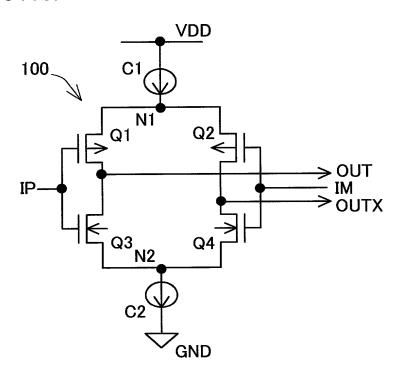


FIG. 26A PRIOR ART

ANOTHER DIFFERENTIAL SIGNAL OUTPUT CIRCUIT ACCORDING TO PRIOR ART

CIRCUIT WITH PASSIVE LOADS

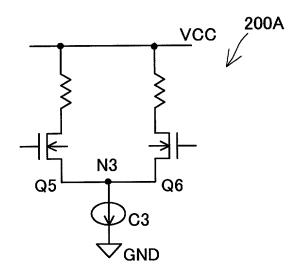


FIG. 26B

CIRCUIT WITH ACTIVE LOADS

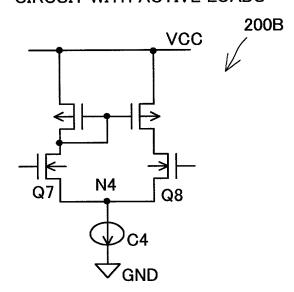


FIG. 27 PRIOR ART

SIGNAL DETECTION APPARATUS ACCORDING TO PRIOR ART

